Amendments to the Drawings

In Fig. 1, a label for the ECC is added in block 103.

Appropriate Replacement Sheet(s) for the amended drawings are submitted herewith.

Remarks

Claims 1-3 and 5-9 are pending in the application. Fig. 1 has been amended in response to an objection to the drawings. Favorable reconsideration of the application, as amended, is respectfully requested.

Applicants note with appreciation the Examiner's continued careful examination of the application.

I. OBJECTION TO THE DRAWINGS

The Examiner objects to the drawings as not showing every feature recited in the claims. Specifically, the Examiner indicates that the drawings do not reflect the case where the data scramble circuit acts as part of an error correction circuit (ECC).

In response, applicants submit herewith a revised Fig. 1. Applicants have amended Fig. 1 to include the ECC circuit and the data scramble circuit as part of a same circuit. No new matter has been added.

In view of the above changes, withdrawal of the objection is respectfully requested.

II. REJECTION OF CLAIMS 1, 3 AND 6-9 UNDER 35 USC §103(a)

Claims 1, 3 and 6-9 now stand rejected under 35 USC §103(a) based on U.S. Patent No. 5,982,887 (*Hirotani*) in view of newly cited U.S. Patent No. 6,907,125 (*Oishi*), and further in view of *Schneier*. Applicants respectfully traverse this rejection for at least the following reasons.

The Examiner has withdrawn the previous rejection of claims 1-3 and 5-9 under 35 USC §103(a) based on *Hirotani*, *Schneier* and *Smith*. However, the Examiner now rejects claims 1-3 and 5-9 under 35 U.S.C. §103(a) based on *Hirotani* and *Schneier* in view newly cited *Oishi*.

The Examiner admits that *Hirotani* does not teach or suggest *a data scramble circuit* being a hardware circuit *and acting as part of an error correction circuit*. Further, *Schneier* is cited for the aspect of teaching that encryption and decryption can be performed in a hardware circuit. However, *Schneier* does not teach that the *data scramble circuit is acting as part of an error correction circuit*.

The Examiner relies on *Oishi* as making up for the deficiencies in *Hirotani* and *Schneier*. Specifically, the Examiner submits that *Oishi* teaches the aspect that error correction can be combined with a decryption system by encrypting error correction codes as well as the stored data and then decrypting the codes and using them in error correction. Applicants respectfully disagree with the Examiner for at least the following reasons.

Independent claims 1, 3, 6 and 8 each recite, *inter alia*, that the *data scramble circuit* is a hardware circuit and *acts as part of an error correction circuit*. As discussed in the specification, any circuit that can perform a reversible data scramble function can be used as the data scramble circuit. In the case where the device includes an error correction circuit, the error correction circuit has a reversible data scramble function and thus can be used as the data scramble circuit (see page 8, lines 3-10 of the specification). Thus, data scramble and error correction can be implemented using a single circuit.

Oishi describes an apparatus for processing information including an error correcting coding device and an encryption device. As can be seen in Fig. 1 of *Oishi*, the error correcting coding device and encryption coding device are implemented in different circuits (i.e., ECC circuit 4 and encryption circuit 5). Moreover, *Oishi* clearly describes the ECC circuit 4 and the encryption circuit 5 as being separate circuits (see, e.g., col. 4, lns. 21-25 and col. 5, lns. 4-20). The teachings of *Oishi* must be considered as a whole. Thus, the combination of *Hirotani*, *Schneier* and *Oishi* would result in a circuit having *individual encryption and error correcting circuits*.

Oishi simply does not teach or suggest that a data scramble circuit acts as part of an error correction circuit, as recited in the independent claims 1, 3, 6 and 8. Rather, *Oishi* teaches directly away from such a combination by teaching that the error correcting coding device and the encryption coding device are implemented in different circuits. It is well settled that the teachings of a reference must be considered as a

whole. The Examiner cannot pick and choose from the teachings of *Oishi* and argue that it would have been obvious from *Oishi* to combine a data scramble circuit as part of an error correction circuit, particularly when other teachings of *Oishi* teach the complete opposite.

Accordingly, it would not have been obvious to a person having ordinary skill in the art to combine the teachings of *Hirotani*, *Schneier* and *Oishi* in the manner suggested by the Examiner. The teachings of Oishi teach completely away from such a combination as noted above. Therefore, the references do not teach or suggest all the features of independent claims 1, 3, 6 and 8 as claimed and, therefore, the rejection under 35 USC §103(a) is improper.

For at least the above reasons, withdrawal of the rejection is respectfully requested.

II. REJECTION OF CLAIMS 2 AND 5 UNDER 35 USC §103(a)

Claims 2 and 5 stand rejected under 35 USC §103(a) based on U.S. Patent No. 5,982,887 (*Hirotani*) in view of newly cited U.S. Patent No. 6,907,125 (*Oishi*), *Schneier*, and further in view of *Oualline* and *Ooi et al.* Applicants respectfully traverse this rejection for at least the following reasons.

Claims 2 and 5 depend from one of the above independent claims and, therefore, can be distinguished from the cited art for at least the same reasons.

Accordingly withdrawal of the rejection of claims 2 and 5 is respectfully requested.

III. CONCLUSION

Accordingly, claims 1-3 and 5-9 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Serial No. 09/754,018

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

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